E5 cont

a third impurity region and a fourth impurity region formed within said semiconductor substrate, wherein said third impurity region is deeper than said fourth impurity region;

wherein said first and third impurity regions are formed in a common impurity region of the semiconductor substrate;

wherein the depth of the second and fourth impurity regions is not larger than 0.1 μm.

REMARKS

At the outset, the Examiner is thanked for the review and consideration of the present application. Additionally, the Examiner is thanked for indicating that claims 1-10, 20-24, 26, 27, 30, 33-35, 37, 39, 42-44, 46, 48, 51-53, 55, 57, 60, 61, 63-65, 69, 70, 72-74, 78, 79, 81-83, 87, 88, 90-92, 96, 97, 99-101, 105, 106, 108-110, 113-115, 118-120, 122, 124, 126, 127, 129, 130, 132, 133, 135, 136, 138, 139, 141, 142, 144, 145, 147, 148, 150, 151, 153, and 154 are allowed over art of record, and that claims 116, 117, 121, 123, and 125 are objected to as dependent on a rejected base claim but would be allowable if each were put in completed form as independent claims, including claim limitation of claims 17, 116; 18, 117; 25, 121; 28, 123; and 112, 125.

The Examiner's Final Office Action dated July 5, 2001 has been received and its contents reviewed. By this Amendment, claims 116, 117, 121, 123, and 125 have been canceled, and claims 17, 18, 25, 28, and 112 have been amended in accordance with the Examiner's recommendation. Accordingly, claims 1-10, 17-115, 118-120, 122, 124, and 126-154 are pending in the present application, of which claims 1, 3, 5, 7, 9, 17, 18, 20, 22, 24, 25, 26, 28, 30, 112, 113, and 115 are independent.

Referring now to the Office Action, claims 17-19, 25, 28, 29, 31, 32, 36, 38, 40, 41, 45, 47, 49, 50, 54, 56, 58, 59, 62, 66-68, 71, 75, 103, 104, 107, 111, 112, 128, 131, 134, 137, 140, and 152 are rejected under 35 U.S.C. § 102(b) as allegedly unpatentable over Komori et al. (U.S. Patent No. 4,972,371); claims 76, 77, 80, 84-86, 89, 93-95, 98, 102, 143, 146, and 149 are rejected as allegedly under 35 U.S.C. § 103(a) as allegedly unpatentable over Komori et al. in view of Chou of record; and, claims 116, 117, 121, 123, and 125 are objected to as dependent

upon a rejected claim. These rejections and objection are respectfully traversed at least for the reasons provided below.

Independent claims 17, 18, 25, 28, and 112 have been amended to include the allowable features of claims 116, 117, 121, 123, and 125, respectively, as shown above. Accordingly, claims 116, 117, 121, 123, and 125 have been canceled. Therefore, independent claims 17, 18, 25, 28, and 112 and their respective pending dependent claims are now contain allowable features.

In view of the amendments and arguments set forth above, the §102(b) and §103(a) rejections are respectfully requested to be reconsidered and withdrawn.

CONCLUSION

Having responded to all rejections set forth in the outstanding Final Office Action, it is submitted that claims 17-19, 25, 28-29, 31-32, 36, 38, 40-41, 45, 47, 49-50, 54, 56, 58-59, 62, 66-68, 71, 75-77, 80, 84-86, 89, 93-95, 98, 102-104, 107, 111-112, 128, 131, 134, 137, 140, 143, 146, 149, and 152 are now in condition for allowance, as well as claims 1-10, 20-24, 26, 27, 30, 33-35, 37, 39, 42-44, 46, 48, 51-53, 55, 57, 60, 61, 63-65, 69, 70, 72-74, 78, 79, 81-83, 87, 88, 90-92, 96, 97, 99-101, 105, 106, 108-110, 113-115, 118-120, 122, 124, 126, 127, 129, 130, 132, 133, 135, 136, 138, 139, 141, 142, 144, 145, 147, 148, 150, 151, 153, and 154. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of

the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,

By_____

Eric J. Robinson
Reg. No. 38,285

NIXON PEABODY, LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
Telephone: (703) 790-9110
Facsimile: (703) 883-0370

EJR:LCD:sbs

VERSION OF AMENDED ABSTRACT WITH MARKINGS TO SHOW CHANGES MADE

A semiconductor memory device including a first memory having a first floating gate formed over a semiconductor substrate, a first control gate formed over and insulated from the first floating gate, a first impurity region and a second impurity region formed within the semiconductor substrate, wherein the first impurity region is deeper than the second impurity region, and a second memory having a second floating gate formed over the semiconductor substrate, a second control gate formed over and insulated from the second floating gate, the first impurity region, and a third impurity region formed within said semiconductor substrate, wherein the first impurity region is deeper than said third impurity region, and a pair of wirings [functioning as a bit line] formed on and in electrical contact with the second and third impurity regions, respectively. In one embodiment, the pair of wirings may function as a bit line.

VERSION OF AMENDED CLAIMS WITH
MARKINGS TO SHOW CHANGES MADE

17. (Amended) A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region;

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

said first impurity region; and

a third impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said third impurity region;

wherein the depth of the second and third impurity regions is not larger than 0.1 μm.

18. (Amended) A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region;

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

said first impurity region; and

a third impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said third impurity region, and

a wiring formed on and in electrical contact with said first impurity region;

wherein the depth of the second and third impurity regions is not larger than 0.1 μm.

25. (Amended) A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, said first impurity region being deeper than said second impurity region, wherein said first impurity region is partly overlapped with said first floating gate; and

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

said first impurity region; and

a third impurity region formed within said semiconductor substrate, said first impurity region being deeper than said third impurity region, wherein said first impurity region is partly overlapped with said second floating gate;

wherein the depth of the second and third impurity regions is not larger than 0.1 μm.

28. (Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a floating gate formed over said semiconductor substrate;

a control gate formed over and insulated from said floating gate;

a first impurity region and a second impurity region formed within said semiconductor substrate, said first impurity region being deeper than said second impurity region, wherein said first impurity region is partly overlapped with said floating gate;

an interlayer insulating film formed over said semiconductor substrate, said floating gate and said control gate; and

a wiring formed on said interlayer insulating film wherein said wiring is electrically connected to said first impurity region through a hole formed in said interlayer insulating film;

wherein the depth of the second impurity region is not larger than 0.1 μm.

112. (Amended) A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region;

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

a third impurity region and a fourth impurity region formed within said semiconductor substrate, wherein said third impurity region is deeper than said fourth impurity region;

wherein said first and third impurity regions are formed in a common impurity region of the semiconductor substrate;

wherein the depth of the second and fourth impurity regions is not larger than 0.1 μm.